Airbridge Gate FET[1] for GaAs Monolithic Circuits

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Abstract—**This paper describes a novel technology for producing micron- and submicron gate FET devices with improved gain and noise performances.**

The technique is particularly attractive for the production of very low-noise devices and is very useful in monolithic circuit fabrication.

In the production of high-power devices, the technique has the advantage of not requiring complicated interdigitated structures. A noise figure improvement of 0.4 dB at 10 GHz was achieved using this technology. As an example of the developed technique, a two-stage monolithic preamplifier (2.8-dB NF, 15-dB gain between 11.7 and 12.5 GHz) is described.

This amplifier was connected with other monolithic circuits to form a multichip DBS front-end receiver having 43 ± 2.5 dB conversion gain and 4-dB NF_{MAX}.

I. Introduction

IT IS WELL KNOWN that the noise and gain performances of FET devices can be enhanced by reducing the device gate length [1], [2].

The good performances, for a given gate length, are strictly related to the reduction of the distributed gate resistance R_g and of the source resistance R_s.

For this reason, it is important to set up a simple high-yield process to realize monolithic circuits where the active devices have very low gate and source resistances. The source resistances of discrete devices are frequently reduced using recessed gate structures. However, because of the complications inherent in the process, this choice is rather unpractical. An allowable way of reducing the device source resistance is the use of n^+ contacts under the source and drain metallizations. This can be obtained easily through selective ion implantation. On the other hand, some technological limits exist in reducing the gate metallization resistance. The increase in the gate metallization thickness is limited by the difficulty of the submicron line definition. A viable alternative is the T-bar gate device, which may introduce complications in monolithic circuit fabrication. Strong decrease in the single gate arm width requires complicated interdigitated structures (especially for power FET structures).

This paper will first describe a novel technique to construct FET devices with improved noise and gain performances without the need for reducing their gate length.

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[1]TELETTRA patent pending.

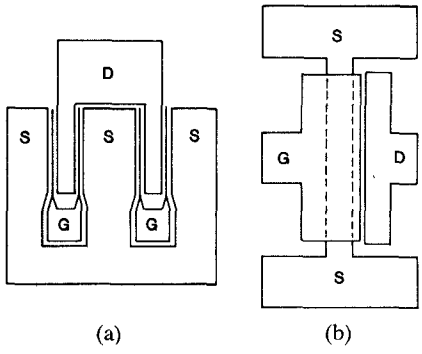

Fig. 1. (a) Conventional FET structure. (b) Airbridge gate FET structure.

Afterwards, a new monolithic low-noise amplifier with airbridge FET's is described, which operates in the 11.7–12.5-GHz band with 15-dB gain and 2.8-dB NF.

A brief description follows of other monolithic circuits, which were connected to such an amplifier to form a multichip DBS front-end receiver. The front-end consists of the low-noise amplifier, a dual-gate mixer, an IF amplifier, and a high-stability local oscillator. Test results and RF yield will be reported for each developed circuit. Finally, the performances of the multichip front-end will be described.

II. The Airbridge FET Technology

In order to explain the new device structure easily, Fig. 1(a) and (b) show the conventional FET structure and the airbridge gate FET, respectively. In the new structure, the gate electrode consists of an airbridge connection over the source electrode. The airbridge connects the gate pad at one side of the source strip contact, and the gate electrode along its whole width at the other side. In Fig. 2, the cross section of the structure is shown.

In this way, a much lower metalization resistance can be attained in comparison with the conventional gate structure in Fig. 1(a). For example, the gate resistance of the Fig. 1(a) FET having an aluminum gate 500-μm wide and 0.4-μm high, is reduced from 2.6 to 3.2×10^{-4} Ω. So small values of the gate resistance cannot be obtained when the T-bar gate cross section is used.

The technology to achieve this structure is quite similar to the well-known airbridge technology and is well suited to the monolithic circuit fabrication.

In Fig. 3, an example of the technological process is shown.

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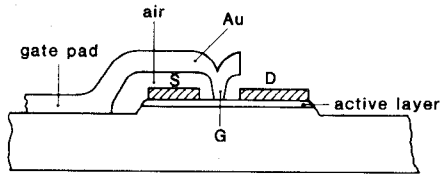

Fig. 2. Cross section of an airbridge gate FET.

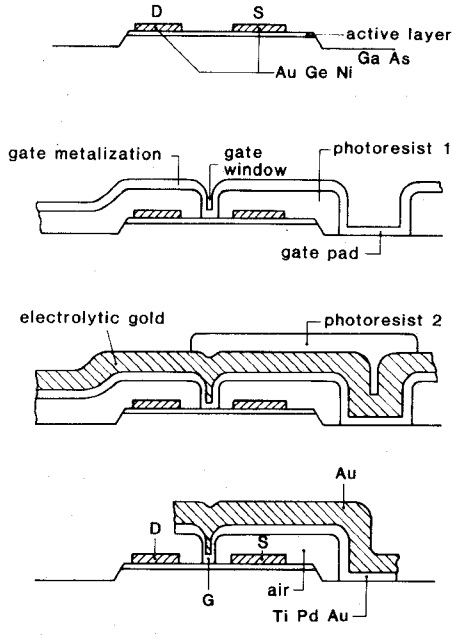

Fig. 3. Airbridge gate technology.

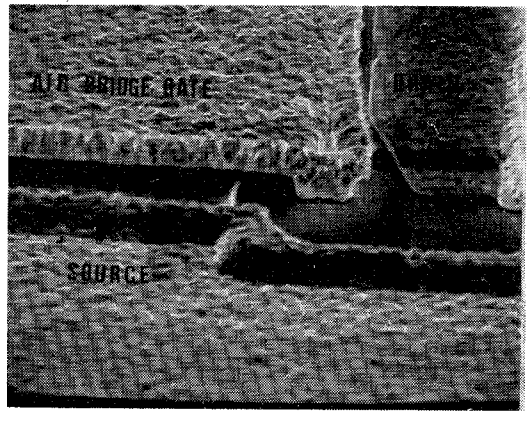

Fig. 4. Scanning electron micrograph of an airbridge gate.

Starting from the source and drain pads (Fig. 3(a)), the gate length and the gate pads are defined by standard conventional photolitography. Afterwards, a gate metalization is evaporated over the whole wafer (Fig. 3(b)). Electrolytic gold is successively grown on the gate metalization ($t \simeq 3 \div 4$ μm) and a second photoresist layer is deposited and masked to define the airbridge connection (Fig. 3(c)). Finally, the electrolytic gold and the gate metalization are etched-off through the photoresist mask and the two photoresist layers are removed to get the wanted structure in Fig. 3(d).

The air gap is about 4-μm high and involves a negligible parasitic capacitance toward the source. Fig. 4 shows a scanning electron micrograph of an airbridge gate structure.

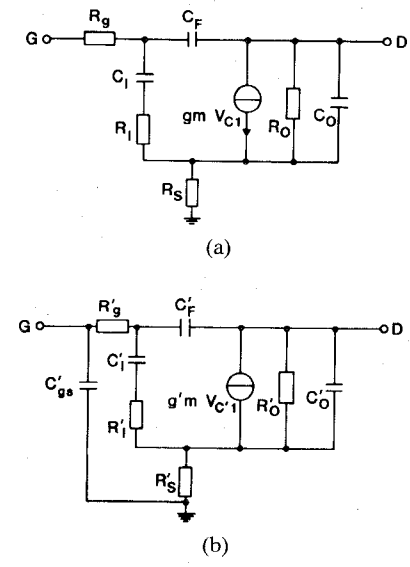

Fig. 5. (a) Equivalent circuit of the FET in Fig. 1(a). (b) Equivalent circuit of the FET in Fig. 1(b).

Obviously, instead of a continuous bridge along the gate, a structure with parallel bridge strips can be realized, which can drastically reduce the distributed gate resistance too, but which introduces lower parasitic capacitance versus the other FET electrodes. To reduce the parasitic inductance to ground, the source contact is grounded through via-holes.

In order to evaluate the impact of the new structure on the device gain and noise performances, suppose that, with the same process, we construct two FET's, one very near the other, on the same doped GaAs substrate. The first FET (FET 1) has the topology in Fig. 1(a), while the second (FET 2) has the topology in Fig. 1(b). We impose that the following parameters are equal in both cases: Z = total gate width, L = gate length, L_{GS} = gate–source spacing, L_{GD} = gate–drain spacing.

In Fig. 5(a) and (b), the equivalent circuit is reported for FET 1 and FET 2, respectively. Most of the circuit parameters in Fig. 5(b) can be assumed to be nearly equal to those in Fig. 5(a) since they are essentially determined by the material and the processing: $C_I \simeq C'_I$, $R_I \simeq R'_I$, $R_s \simeq R'_s$, $R_0 \simeq R'_0$, $g_m \simeq g'_m$. Obviously, $R'_g \ll R_g$ and $C'_F = C_F + \Delta C_F (\Delta C_F > 0)$, $C'_0 = C_0 + \Delta C_0$.

For a source linewidth of 20 μm, the parasitic capacitance C'_{gs} between the gate and the source contact of FET 2 can be calculated as a parallel-plate capacitor, and is $\simeq 4 \times 10^{-2}$ pF per millimeter of gate width.

The increase ΔC_F in the feedback capacitance is mainly due to the field lines between the bridge and the drain on the air side only, since, on the GaAs side, the drain is shielded by the source contact. Such an increase was computer calculated using a spectral-domain Galerkin method [3] and is about 1.4×10^{-2} pF per millimeter of gate width.

C'_0 can be evaluated easily as a proximity capacitance [1] between the source and drain metals and is mainly due to the field lines in the GaAs side.

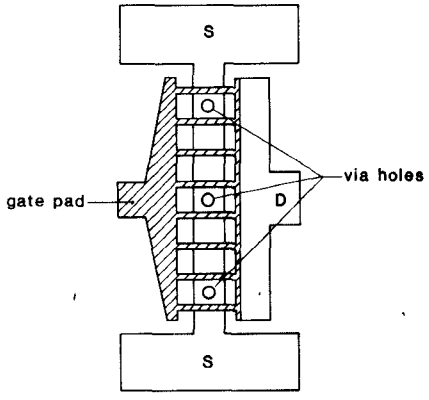

Fig. 6. Comb-bridge gate FET

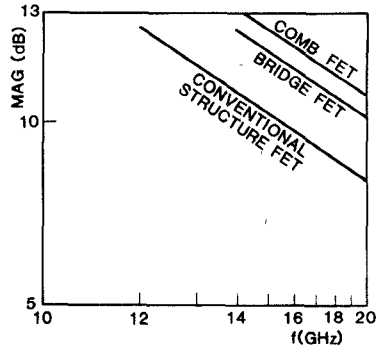

Fig. 7. Maximum available gain (MAG) for FET's of different structures.

TABLE I

	TOPOLOGY	n^+ CONTACTS	Z (mm)	z (mm)	N (cm^{-3})	L (μm)	$L_{GS} = L_{GD}$ (μm)	h (μm)	a (μm)	NF_{MIN} (dB) f = 10 GHz
FET 1	fig. 1a	no	0.3	0.075	$2.5\ 10^{17}$	0.5	1	0.2	0.2	2.35
FET 2	fig. 1a	no	0.3	0.075	$2.5\ 10^{17}$	0.5	1	0.4	0.2	2.0
FET 3	fig. 1b	no	0.3	--	$2.5\ 10^{17}$	0.5	1	--	0.2	1.7
FET 4	fig. 1a	yes	0.3	0.075	$2.5\ 10^{17}$	0.5	1	0.2	0.2	2.15
FET 5	fig. 1a	yes	0.3	0.075	$2.5\ 10^{17}$	0.5	1	0.4	0.2	1.8
FET 6	fig. 1b	yes	0.3	--	$2.5\ 10^{17}$	0.5	1	--	0.2	1.4

On the basis of the above circuit considerations, it can be shown easily that the reduction of R_g results into a gain advantage of FET 2 over FET 1, but simultaneously it produces a shift toward the higher frequencies of the device potential instability ($K<1$). The simultaneous increase of the feedback capacitance also contributes to such an effect, but it limits the gain advantage.

This limit can be overcome by considering, instead of a full bridge, the comb-bridge structure in Fig. 6. The experimental effect on the device MAG of the different structures (Fig. 1(a) and (b) and 6) is shown in Fig. 7. The following parameters were chosen: doping density $N = 2.5 \cdot 10^{17} cm^{-3}$, $Z = 500$ μm, $L = 0.5$ μm, $L_{GD} = L_{GS} = 1$ μm, $n^+ = 3 \times 10^{18}\ cm^{-3}$.

For the device in Fig. 1(a), the gate height was $h = 0.4$ μm, and for the device in Fig. 7, the bridge was substituted by seven strips, 5-μm wide.

In Table I, the calculated [2], [4] minimum noise figures NF_{MIN} for different FET's are reported. As can be seen by comparing FET 3 in the table with FET's 4 and 5, in terms of reduction of the minimum noise figure, the airbridge approach is more effective than the n^+ contact approach. A minimum noise figure of 1.4 dB at 10 GHz is expected for a 0.5-μm gate length device having both airbridge gate and n^+ contacts.

The substantial adequacy of the above analysis was experimentally confirmed. To this purpose, FET devices having parameters very similar to those of FET 5 and FET 6 in Table I were tested. For the conventional structure devices (No. 5), minimum noise figures at 10 GHz between 1.85 and 1.95 dB were measured. For the airbridge devices, the measured NF_{MIN} values turned out to be between 1.45 and 1.55 dB, thus giving a mean reduction of ~ 0.4 dB.

III. The Airbridge Monolithic Amplifier

The airbridge technology was used to construct a low-noise amplifier working in the 11.7–12.5-GHz band.

The amplifier makes use of two 0.5-μm gate FET's with n^+ contacts under the source and drain electrodes, which were previously characterized between 1 and 18 GHz, as scattering and noise parameters. The amplifier equivalent circuit is shown in Fig. 8.

The matching circuits basically make use of inductive elements with a stabilizing resistor inserted in the interstage network.

The measured amplifier performances are shown in Fig. 9.

The chip dimensions are 1.1×2.4 mm^2 (Fig. 10). The amplifier yield was 55 percent.

As an example of the technological process, we list the steps for the airbridge amplifier fabrication:

a) realization of active area and resistors by mesa etching,
b) ohmic contact and bottom MOM electrode formation,

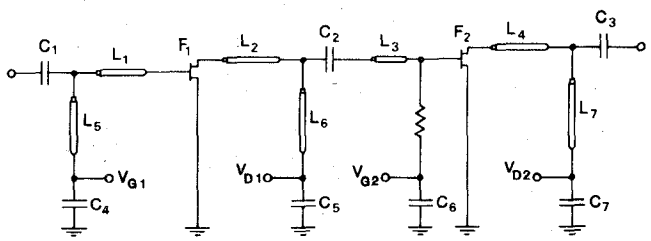

Fig. 8. Equivalent circuit of the monolithic preamplifier.

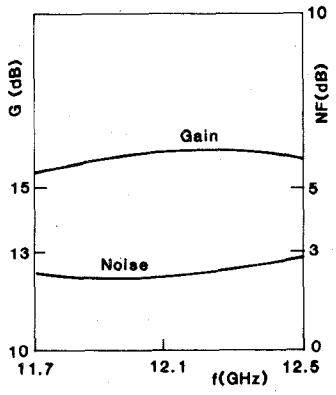

Fig. 9. Performances of the airbridge low-noise amplifier.

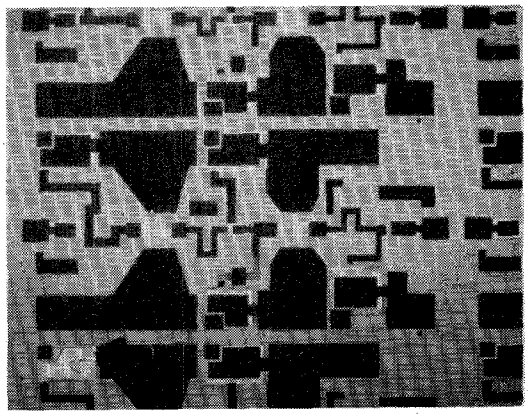

Fig. 10. Airbridge FET monolithic amplifier.

c) polymide overcoat and dielectric area definition,
d) gate and passive circuit delineation,
e) airbridge formation both for gates and connections on top MOM electrodes.

As can be seen, there is no difference with respect to the conventional monolithic fabrication; in fact, in step e), we construct the airbridge connection for the MOM capacitors (a widely used technique) at the same time as the airbridge gates for the FET's.

IV. The Multichip Monolithic Front-End Receiver

In order to obtain experimental evidence of the impact of the described technology on the performances of a complete subsystem, a multichip front-end receiver was constructed and tested. The front-end consisted of four basic functions: preamplifier, mixer, local oscillator, and IF amplifier. As preamplifier, use was made of the above-described low-noise amplifier.

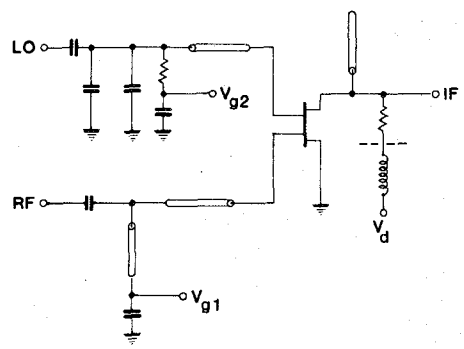

Fig. 11. Equivalent circuit of the dual-gate mixer.

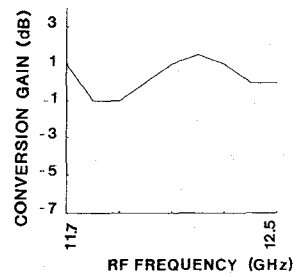

Fig. 12. The mixer conversion gain versus frequency.

A. Mixer

A gainy mixer solution was chosen in order to optimize the overall front-end noise and gain performance. A dual-gate FET was selected as the active element to avoid the need for complex and large-size circuits, such as couplers and isolation filters. Since a matching IF circuit is unpractical both for bandwidth and size reasons, an unusual but efficient high-impedance output solution was adopted by directly connecting the dual-gate mixer with the input of the IF amplifier. Quite a high (~10 dB) mixer noise figure was measured at one single frequency by connecting the IF output to a load impedance equal to the input impedance of the IF amplifier. The reason for this NF value was the power loss due to the unmatched mixer output.

A second important feature of the mixer is the choice of reactively loading the local oscillator input (gate 2) at the RF signal frequencies, since it was experimentally noticed that this solution, which enhances the RF dual-gate gain, optimizes the conversion gain too. An unmatched (reflecting) load was therefore chosen for the line of the local oscillator, the required optimum power level being quite low (4 dBm).

In Fig. 11, the electric circuit of the mixer is reported. An image rejection filter, matched at 12.1 GHz is connected with the RF input (gate 1). On the drain output, a shunt open stub acts as LO and RF filter.

Gates 1 and 2 are biased through a parallel line and a 1-kΩ mesa resistor, respectively, while the drain is biased through an external inductance that is the only external bias network necessary for the whole front-end.

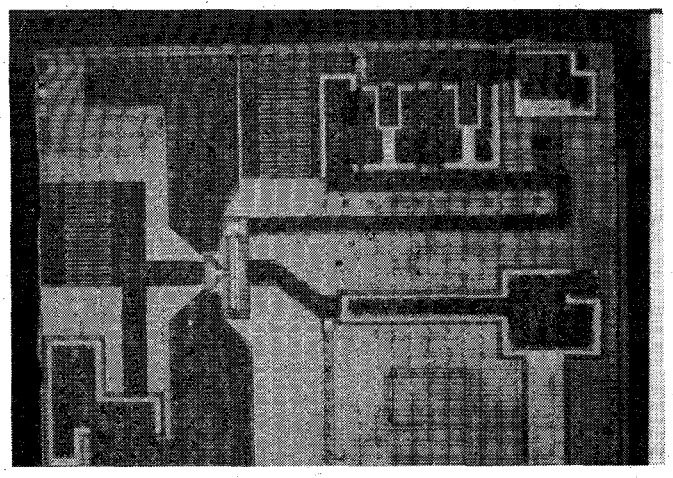

Fig. 13. The mixer chip.

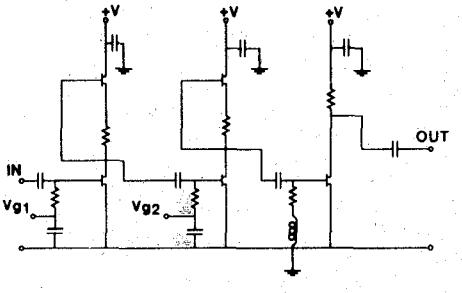

Fig. 14. Equivalent circuit of the IF amplifier.

In Fig. 12, the typical mixer performance is reported.

A photograph of the mixer chip is reported in Fig. 13. The chip area is 2.5×1.9 mm^2. The overall RF yield is 85 percent.

B. IF Amplifier

An IF amplifier that does not require external biasing elements (chokes, capacitors) was selected. As shown in its electric circuit in Fig. 14, an FET drain bias through self-biasing active loads was chosen in order to simultaneously achieve small size and reduced power consumption. FET devices with 200- , 400- , and 600-μm gate widths were used for the first, second, and third stage, respectively. The in-band gain flatness is obtained by means of an equalizing $R-L$ circuit that shunts the input of the third stage.

The amplifier gain and the output return loss measured in a 50-Ω test jig are reported in Fig. 15. The measured noise figure is lower than 4.5 dB. The power consumption is maintained below 0.7 W. The dimensions of the chip shown in Fig. 16 are 3.4×1.7 mm^2; its RF yield is over 47 percent.

C. Local Oscillator

An original solution using a dielectric resonator coupled with a monolithic oscillator through a coplanar waveguide was developed. The design procedure as well as the performances of the developed monolithic oscillators are published elsewhere [5]. In the case of the monolithic DBS front-end, a 0.8-μm $\times$ 450-μm gate FET is used. The output

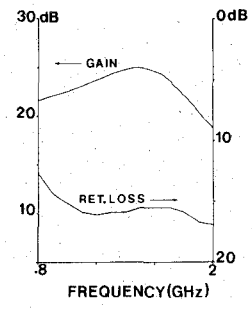

Fig. 15. Performances of the IF amplifier.

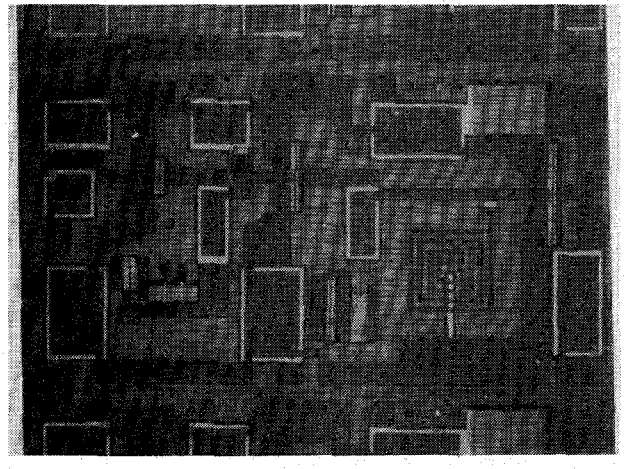

Fig. 16. The IF amplifier chip.

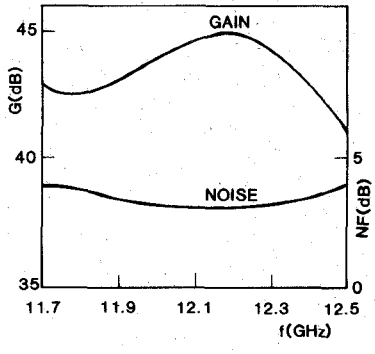

Fig. 17. The performances of the multichip DBS front-end receiver.

level is 7 dBm at the frequency of 10.75 GHz. The measured thermal drift is 6.5 ppm/°C, the external Q factor is 3000, and the pushing figure is 150 kHz/V. The circuit RF yield is 88 percent.

In Fig. 17, the measured performances for the multichip DBS receiver are shown: a conversion gain of 43 ± 2.5 dB and 4-dB NF_{MAX} were obtained.

IV. Conclusions

A new technology for producing FET devices with improved noise and gain performances without reducing the device gate length has been described. A low-noise monolithic amplifier having 15-dB gain and 2.8-dB NF_{MAX} has been described. The design and performances of a multichip DBS front-end receiver with 43 ± 2.5-dB gain and 4-dB NF have been reported.

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In 1967, he joined CISE, Center for Information, Studies, and Experiments, at Segrate (Milan), where he was first engaged in the development of high-speed logic circuits and is now working on GaAs microwave devices and subsystems. Since 1976, he has been the responsible for the CISE Microwave Section.

Giampiero Donzelli was born in Milan, Italy, on March 27, 1949. In 1975, he received the degree of doctor in physics (electronic branch) from the Physic Institute of Milan (Italy).

In 1968, he joined CISE-Segrate (Milan), where he was involved in GaAs technology related to the optoelectronic-devices field (double heterostructure lasers). Since 1976, he has been working on research and development of GaAs MESFET's and integrated-circuit technology for microwave applications. In 1983, he joined TELETTRA, where he is responsible for research and development of microwave GaAs devices and circuits. His major contributions are in the field of GaAs material characterization, device technology development, and realization of new microwave circuits.